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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHAUHAN, ULKA J	

ART UNIT	PAPER NUMBER
2676	20

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/397,188	GRIGOR ET AL.	
	Examiner	Art Unit	
	Ulka J. Chauhan	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-24* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/18/04 has been entered.

2. Claims 21-24 are newly added; claims 1-24 are pending.

3. The indicated allowability of claims 1-10, 15, and 16, is withdrawn in view of the newly discovered reference(s) to Brothers. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-9, 11-15, and 17-24 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,128,026 to Brothers, III.

6. As per claim 1, Brothers teaches a write blocking accelerator 200 coupled to a computer system in which 2D and 3D engines 220 receive commands (*receiving a rendering command*) from the CPMC 218, and generate display data that will subsequently be used to update a location on the display 228 by writing this data to the frame buffer 230 after receiving an

acknowledgement from the memory interface unit, MIU 222 (*rendering an image based upon the rendering command, wherein the image is to be stored at a first memory location of a first frame buffer*) [c. 5 ll. 16-19, ll. 37-45, and Fig. 2]. Brothers discloses that the screen refresh unit, SRU 226, sets the values in a last address register 232 for storing the starting address of the line after the last line within the current front buffer 230A, and a next address register 234 for storing the starting address of the data corresponding to the next scan line to be displayed (*determining a second memory location representative of a raster location*), which are utilized while operating in a write blocking mode [c. 6 ll. 1-7 and ll. 37-45]. Brothers discloses that the memory interface unit, MIU 222, which controls the 2D and 3D engines' access to the frame buffer, checks the address ranges of the write requests received from the engines 220 against the next address value received from the SRU 226, and allows writes to addresses behind the blocked range--that is, writes directed to addresses for which display data has already been transferred to the display 228 (*enabling, by a write behind controller in a video graphics adapter, storage of the image at the first memory location when the second memory location indicates the raster has accessed data at the first memory location*) [c. 6 ll. 53-64]. And Brothers discloses that if an engine 220 attempts to write to an address within the blocked address range, the MIU 222 preferably waits until the SRU 226 issues or provides a next address value that exceeds or lies beyond the addresses to which the engine 230 will write, after which the MIU 222 provides a handshaking signal to the engine 220, thereby allowing the engine to write to the front buffer 230A (*preventing, by the write behind controller, storage of the image at the first memory location when the second memory location indicates the raster has not accessed data at the first memory location*) [c. 6 ll. 65-c. 7 ll. 5].

7. As per claim 2, Brothers discloses that the CPU 210 sends drawing commands to the accelerator 200 [c. 4 ll. 16-26].

8. As per claims 3-5, Brothers discloses that graphical display data from the 2D and 3D engines are intended for any given location on the display 228 and may also include horizontal strips of data [c. 5 ll. 16-29]. And Brothers discloses that the next address register 234 stores the starting address of the data corresponding to the next scan line to be displayed [c. 6 ll. 5-7].

9. As per claim 6 and 7, Brothers discloses that the SRU 226 transfers current image data from the frame buffer 230 to the display, and the next address register 234 stores the starting address of the data corresponding to the next scan line to be displayed [c. 5 ll. 57-59 and c. 6 ll. 5-7]. And Brothers discloses that a current address register which would store the starting address of the data corresponding to the current scan line being displayed, rather than the next address register 234 could be utilized [c. 6 ll. 7-12].

10. As per claim 8, Brothers teaches a write blocking accelerator 200 coupled to a computer system in which 2D and 3D engines 220 receive commands from the CPMC 218, and generate display data that will subsequently be used to update a location on the display 228 by writing this data to the frame buffer 230 after receiving an acknowledgement from the memory interface unit, MIU 222 [c. 5 ll. 16-19, ll. 37-45, and Fig. 2]. Brothers discloses that the 2D and 3D engines 220 respectively process 2D and 3D drawing commands where graphical display data is intended for any given location on the display 228 and may also include horizontal strips [c. 5 ll. 9-28]. Therefore Brothers implicitly teaches *defining a graphics primitive having a first portion at X and a second portion at Y, wherein X and Y are indicative of address locations.* The 2D and 3D engines 220 write display data to the frame buffer 230 while the screen refresh unit, SRU

226, transfers current image data from the frame buffer 230 to the display 228 (*the rendering engine is storing data to a frame buffer being accessed by a display device controller providing a current image*) [c. 5 ll. 56-59]. The writes to the frame buffer 230 occur behind the scan line, whereby writes to the undisplayed portion of the frame buffer 230 are prevented, thereby preventing the occurrence of discontinuities or artifacts in the displayed image (*where the display device controller is yet to access an address location Z having data associated with the current image and the location Z is between X and Y*) [c. 5 ll. 59-65]. Brothers further discloses that the 2D and 3D engines 220 process as many commands as possible without writing ahead of the scan line (*providing the graphics primitive to a rendering engine*), thereby ensuring that the displayed image remains unaffected (*preventing tearing of the current image*) [c. 7 ll. 17-20].

11. As per claim 9, Brothers discloses that the 2D and 3D engines 220 respectively process 2D and 3D drawing commands where graphical display data is intended for any given location on the display 228 [c. 5 ll. 9-28]. Therefore, Brothers implicitly teaches address locations include *display line numbers*.

12. As per claims 11 and 12, Brothers teaches a write blocking accelerator 200 coupled to a computer system in which 2D and 3D engines 220 receive commands from the CPMC 218, and generate display data that will subsequently be used to update a location on the display 228 by writing this data to the frame buffer 230 after receiving an acknowledgement from the memory interface unit, MIU 222 [c. 5 ll. 16-19, ll. 37-45, and Fig. 2]. Brothers discloses that the 2D and 3D engines 220 respectively process 2D and 3D drawing commands where graphical display data is intended for any given location on the display 228 and may also include horizontal strips [c. 5 ll. 9-28]; therefore, Brothers implicitly teaches *image primitive*. The 2D and 3D engines

220 write display data to the frame buffer 230 while the screen refresh unit, SRU 226, transfers current image data from the frame buffer 230 to the display 228 (*storing a first portion of an image primitive to the first portion of the frame buffer after the step of displaying the first portion of video/graphics data*) [c. 5 ll. 56-59], such that the writes to the frame buffer 230 occur behind the scan line, whereby writes to the undisplayed portion of the frame buffer 230 are prevented, thereby preventing the occurrence of discontinuities or artifacts in the displayed image (*prohibiting, by a write behind controller in a video graphics adapter, a second portion of the image primitive from being stored to a second portion of the frame buffer after the step of storing the first portion, wherein the second portion of the frame buffer is adjacent to the first portion of the frame buffer* and *storing the second portion of the image primitive to the second portion of the frame buffer after the step of accessing the second portion of the video/graphics data*) [c. 5 ll. 59-65]. Brothers further discloses that the 2D and 3D engines 220 process as many commands as possible without writing ahead of the scan line thereby ensuring that the displayed image remains unaffected [c. 7 ll. 17-20].

13. As per claim 13, Brothers teaches a write blocking accelerator 200 (*a write behind raster controller*) coupled to a computer system (*a rendering engine to render images*) in which 2D and 3D engines 220 receive commands from the CPMC 218, and generate display data that will subsequently be used to update a location on the display 228 by writing this data to the frame buffer 230 after receiving an acknowledgement from the memory interface unit, MIU 222 [c. 5 ll. 16-19, ll. 37-45, and Fig. 2]. The 2D and 3D engines 220 write display data to the frame buffer 230 while the screen refresh unit, SRU 226, transfers current image data from the frame buffer 230 to the display 228 [c. 5 ll. 56-59], such that the writes to the frame buffer 230 occur

behind the scan line, whereby writes to the undisplayed portion of the frame buffer 230 are prevented, thereby preventing the occurrence of discontinuities or artifacts in the displayed image (*prohibit write access to memory location that have not been displayed*) [c. 5 ll. 59-65].

14. As per claim 14, Brothers discloses that the screen refresh unit, SRU 226, sets the values in a next address register 234 for storing the starting address of the data corresponding to the next scan line to be displayed (*a display device controller coupled to the write behind raster to indicate a raster location*), which are utilized while operating in a write blocking mode [c. 6 ll. 1-7 and ll. 37-45].

15. As per claim 15, Brothers discloses that the SRU 226 sets the values in the last and next address registers 232, 234 (*the rendering engine location register is to store a first memory location to be accessed by the rendering engine*); signals the MIU 222 to enter write blocking mode; and provides the MIU 222 with the contents of the next address register 234(*receive a raster location indicator*); and continues to transfer display data from the frame buffer 230 to the display 228 [c. 6 ll. 37-45]. The MIU 222 checks the address ranges of the write requests received from the engines 220 against the next address value received from the SRU 226, where writes to addresses behind the blocked range--that is, writes directed to frame buffer addresses for which display data has already been transferred to the display 228--are allowed to proceed 324, and prohibits writes into addresses beyond that specified by the next address value (*prohibit the rendering engine from write accessing to memory locations*) [c. 6 ll. 53-64]. If an engine 220 attempts to write to an address within the blocked address range, the MIU 222 preferably waits until the SRU 226 issues or provides a next address value that exceeds or lies beyond the addresses to which the engine 230 will write, after which the MIU 222 provides a handshaking

signal to the engine 220, thereby allowing the engine to write to the front buffer 230A [c. 6 ll. 65-c. 7 ll. 4]. Therefore the absence of the handshaking signal is an implicit *over-run detect indicator*.

16. Claims 17 and 21-24 are similar in scope to claims 1, 8, 11, and 13, and are rejected under the same rationale.

17. As per claims 18, 19, and 20, Brothers discloses that if an engine 220 attempts to write to an address within the blocked address range, the MIU 222 preferably waits until the SRU 226 issues or provides a next address value that exceeds or lies beyond the addresses to which the engine 230 will write, after which the MIU 222 provides a handshaking signal to the engine 220, thereby allowing the engine to write to the front buffer 230A [c. 6 ll. 65-c. 7 ll. 4].

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

20. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,128,026 to Brothers, III and U.S. Patent No. 6,205,531 to Hussain.

21. As per claim 10, Brothers does not expressly teach *one of physical and logical address locations*. Hussain discloses, "Modern computer systems typically provide some form of virtual memory environment. In an environment of this type, application processes (and in some cases, system processes) access memory using virtual addresses. The computer system is responsible for translating these virtual addresses into physical addresses within the memory of the computer system. In a typical virtual memory environment, the virtual address space and the physical address space are both divided into fixed size pages. Each virtual address is a combination of a virtual page address and a page offset. Each physical address is a combination of a physical page address and a page offset. Using this system, page addresses may change during address translation, but page offsets remain the same. The computer system maintains a set of data structures, known as page tables, for each process. The page tables provide a per-process mapping between virtual page addresses and physical page addresses. Translation of a virtual address is accomplished by using the page table to find the physical page address that matches the virtual address being translated. The page offset portion of the virtual address being translated is then added to the physical page address to form the complete physical address" [c. 1 ll. 20-44]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the virtual memory environment taught by Hussain in combination with the computer system taught by Brothers in order to take advantage of operating a system in virtual memory that is larger than the physical memory of the system.

Allowable Subject Matter

22. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

23. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

24. The prior art, U.S. Patent No. 6091432 to Diehl and U.S. Patent No. 6097401 to Owen, made of record and not relied upon is considered pertinent to applicant's disclosure.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Ulka Chauhan** whose telephone number is **(703) 305-9651**. The examiner can normally be reached Mon.-Fri. from 9:00 am to 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(703) 308-6829**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

26. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 305-4700.

Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
March 21, 2004